VLSI Training Program

A comprehensive industry-oriented training program designed to prepare engineers for the Semiconductor and VLSI industry.

Detailed Syllabus

Module 0 – VLSI Industry Orientation

- Introduction to VLSI Industry and ASIC Design Flow
- Demo of Digital Design Flow using Cadence Tools
- Overview of EDA Tools used in Industry
- Shell Basics for Engineers
- Domains in the VLSI Design Industry
- Design & Fabrication Overview
- Career Opportunities for Fresh Graduates
- Top Companies in the VLSI Industry

Module 1 – Standard Cell Design & Layout

- Standard Cell Library Design using CMOS Logic
- Schematics, Simulation, and Verification
- TCL Scripting for Automation
- Power Analysis & PDKs
- Stick Diagrams & Layout Techniques
- Layout Failure Mechanisms & Area Estimation
- Floorplanning: 9-Track and 12-Track Cells
- Drive Strength, Logical Effort, Multi-Drive Strength Cells, Multi-Vt Cells
- Physical-Only Cells (Fillers, Taps, Antennas, Decaps, End Caps, Tie Cells)
- Physical Verification (DRC, LVS, Post-Layout Simulations)
- Characterization: LEF, LIB
- Tape-out Collaterals: GDS, Spice Netlist, Model File
- Scope: Apply all above techniques to a library of 500+ cells (logic & sequential)
- Tools Used: Virtuoso Schematic/Layout, Abstract, Liberty, Genus, Innovus, Tempus, Assura/PVS

Module 2 – Foundations for Physical Design

- Device Physics: PN Junction, MOSFETs, I-V Characteristics
- DC Transfer Characteristics
- Semiconductor Manufacturing Flow
- Silicon Manufacturing, Photolithography, Oxide Growth/Removal, Diffusion, Silicon Deposition, Assembly
- CMOS Logic Fundamentals
- Logic Gates, Compound Gates, Pass Transistors, Transmission Gates, Tristates, Multiplexers, Sequential Circuits

Module 3 – Standard Cell – Hands-On

- Design of CMOS Logic Gates

- Schematics & Testbench Generation
- Transient & DC Analysis
- Power Analysis & Drive Strength Testing
- Logical Effort & Optimization
- Layout Design & Verification (DRC, LVS)
- Post-Layout Simulations
- Standard Cell Characterization (LEF, LIB)
- Scope: Implementation for 500+ standard cells (logic & sequential)

Module 4 – Synthesis – Hands-On

- Basics of Synthesis & High-Level Synthesis Flow
- Reading Verilog RTL Files
- Target & Link Libraries, Resolving References
- Reading Hierarchical Designs
- Applying Constraints (SDC)
- Analyze & Elaborate Commands
- Constraining & Compiling RTL
- Generating Post-Synthesis Reports & Outputs

Module 5 – PnR – Hands-On

- Floorplanning
- Core Die Sizing, Macro Placement, Blockages
- Placement Strategies & In-Place Optimization
- Congestion Analysis
- Power Planning
- Scan Chain Insertion & Reordering
- Global Routing & Detailed Routing
- Clock Tree Synthesis (CTS)
- Post-PnR Power Analysis

Module 6 – Static Timing Analysis (STA) & Physical Verification – Hands-On

- Introduction to STA
- Delay Models & Library Analysis
- SDC Constraints for STA
- Path-Based Timing Analysis & Reports
- Timing Exceptions & MMMC Analysis
- Post-Layout STA
- Crosstalk (SI) Analysis
- Sign-off STA & ECO Flow
- Practical STA Debug & Fixes
- Physical Verification (DRC, LVS, ERC, IR Drop, EM Analysis)
- Tools Used: Virtuoso, Liberty, Genus, Innovus, Tempus, Assura/PVS

Module 7 – Project (Capstone)

- Industry-Standard Project
- Application of Complete ASIC Design Flow
- Timing Closure & Sign-off Implementation
- End-to-End Flow Demonstration

Module 8 – SystemVerilog for Verification

- Modules, Ports & Blocks (always/initial)
- Blocking vs Non-Blocking Assignments
- Data Types: Bit-vectors, Integers, Reals, Enums, Arrays, Structures, Classes
- Verification-Oriented Coding Practices
- Interfaces: Ports, Modports, Clocking, Procedural Blocks
- Connecting DUT & Testbench via Interfaces
- Interprocess Communication: Fork-Join, Semaphores, Mailboxes

Module 9 – Verification Component & Architecture Development

- Sequencers: Transaction Generation
- Drivers: Stimulus to DUT
- Monitors: Capturing DUT Activity
- Scoreboards: Checking Expected vs Observed Results
- Agents: Bundling Verification Components
- Building Reusable Verification Environments