VLSI Physical Design Training Program

An intensive hands-on training program covering all stages of the Physical Design flow – from synthesis to sign-off verification.

Detailed Syllabus

Module 1 – Synthesis

- Introduction to Synthesis
- Synthesis Flow
- Constraining Design for Timing, Area & Power
- Understanding Timing Library (.lib) Format
- Design Synthesis Process
- Timing Checks
- Report Generation, Analysis & Debugging
- Optimization Techniques
- Saving & Exporting Results

Module 2 – Floorplanning & Power Routing

- Floorplanning Concepts
- Goals of Floorplanning
- Area Estimation (Square, Rectangle, Rectilinear)
- I/O Placement & Macro Placement
- Channel Width Estimation
- Floorplanning Guidelines
- Power Routing
- Goals of Power Routing
- Types of Power Routing
- Power Rings, Power Mesh, Follow-Pin & Std-Cell Rails

Module 3 – Placement

- Goals of Placement
- Types of Placement
- Pre-Placement (End-Cap, Tap & I/O Buffer Cells)
- Pre-Place & In-Place Optimization
- Congestion & Timing Analysis
- Tie Cells & High-Fanout Net Synthesis (HFNS)
- Scan Chain Reordering
- Regioning, Grouping & Bounds

Module 4 – Timing Analysis & Optimization

- Basic Timing Checks (Setup, Hold, etc.)
- Timing Constraints (SDC)

- Timing Corners & PVT Considerations
- Timing Report Analysis
- Common Causes of Violations
- Optimization & Fix Strategies

Module 5 – Clock Tree Synthesis (CTS)

- Importance of Clock Distribution
- Goals of CTS
- Types of Clock Trees
- CTS Specifications
- Building the Clock Tree
- Analyzing & Fine-Tuning Results
- Best-Practice Guidelines

Module 6 – Routing

- Goals of Routing
- Types of Routing (Global, Detailed)
- Post-Route Optimization
- Fixing Routing Violations (DRC, LVS)
- Crosstalk & Signal Integrity Issues
- Guidelines for Optimum Routing

Module 7 – ECO & Sign-off Checks

- Engineering Change Order (ECO)
- What is ECO?
- Types (Timing & Functional)
- ECO Preparation & Implementation
- Placement & Routing for ECO
- Sign-off Checks
- Timing Closure
- Physical Verification (DRC, LVS, ERC)
- IR Drop Analysis
- Electromigration Analysis
- Crosstalk (SI) Analysis
- Sign-off Timing Analysis
- Logical Equivalence Checking (LEC)

Module 8 – Projects

- Industry-Standard End-to-End Projects
- Hands-on Implementation of Learned Concepts
- Timing Closure & Sign-off for a Complete Design
- Final Evaluation & Best Practices