Custom Layout Training Program

A specialized training program focusing on custom standard cell design, schematic development, and physical layout methodologies for ASIC/SoC design.

Detailed Syllabus

Module 1: Introduction to VLSI Design & CMOS Fundamentals

- **1.1 Introduction to VLSI**
- Overview of VLSI Design
- RC Circuits & CMOS Fundamentals
- R, C, RC, RCVI – Network Problems
- Basic Assignments and Practice Problems
- **1.2 CMOS Technology & Fabrication**
- CMOS Fabrication Process
- MOS Theory and Cross Section
- Process Steps in Fabrication
- Basic Process Details – Lithography, Etching, Deposition, etc.
- Introduction to FinFETs
- **1.3 CAD Tools & Physical Verification**
- Introduction to Linux & Shell Commands
- Introduction to Cadence Tools
- Physical Verification Basics – DRC, LVS, Layout Extraction
- Virtuoso Environment – Layout Editor, Schematic Editor, Assura/PVS for Physical Verification
- MOSFET Layout Design
- Fingers and Multipliers Concept

Module 2: Digital Layout Design & Standard Cell Libraries

- **2.1 Fundamentals of Standard Cell Layouts**
- Basics of Standard Cell Libraries and Digital Layouts
- Inverter VTC (Voltage Transfer Characteristics)
- Concept of Logical Effort
- Logic Gate Layout Design
- **2.2 Layout Representation & Library Building**
- Simplified Layout Representation – Stick Diagrams
- Standard Cell Layout Template & Boundary Conditions
- Library Building – Hands-on Activity

Module 3: Custom Digital Layout Design

- **3.1 Skill Development**
- Basic Skill Programming
- Custom Digital Layout Block Assignments

Module 4: Analog & Mixed-Signal Layout Design

• **4.1 Passive Components in Layouts**
• Resistors – Poly Resistor, N-Well Resistor
• Capacitors – MOS Capacitor, MIM Capacitor
• Inductors
• **4.2 Physical Verification & Parasitic Effects**
• Reading Extracted Netlist and Correlating with Circuit/Layout
• Parasitics in Routing – Capacitance & Resistance Formation
• Impact of Parasitics on Circuit Performance
• Physical Verification in Detail – DRC, Antenna, Density Checks
• LVS Debugging Techniques (Block-Level)
• **4.3 Device Matching & Layout Techniques**
• Matching Techniques for MOSFETs, Capacitors, and Resistors
• Floorplanning and Placement
• Base Layer DRC or Placement DRC
• Power Planning for Block Layouts

Module 5: Submicron Process & Reliability Challenges

• **5.1 Layout Challenges in Advanced Nodes**
• Submicron Process Layout Challenges
• Electromigration and Reliability Issues
• **5.2 Layout-Dependent Effects**
• LDE (Layout Dependent Effects) – LOD, WPE
• ESD Protection Design
• Latchup Prevention and Noise Isolation Techniques
• Guard Rings and Shielding
• FinFET Layout Challenges – DPT, TPT

Module 6: Analog Circuit Design & Layout Practices

• **6.1 Analog Building Blocks**
• Working Principles of Common Analog Blocks
• Differential Pair
• Current Mirrors & Multipliers
• Current Reference (I-Ref), Voltage Reference (V-Ref)
• Voltage Regulators
• **6.2 Advanced Analog Layout Techniques**
• Differential Layout and Symmetry
• Parasitic and Environment Matching
• Power Distribution Challenges in Analog Design
• Best Practices for Fast and Reliable Layout
• **6.3 Analog Layout Practice Blocks**
• Comparator
• Operational Amplifiers (1-Stage, 2-Stage & 3-Stage)
• Bandgap Reference